

## 19.1 Direct-Conversion WCDMA Transmitter with $-163\text{dBc/Hz}$ Noise at $190\text{MHz}$ Offset

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In an FDD WCDMA handset, excessive noise from the transmitter at the RX frequency should not be coupled to the receiver input, because this will degrade its noise figure. A duplexer is used to isolate the transmitter from the receiver. For good efficiency, the duplexer must have low insertion loss from the PA to the antenna, but this means that the isolation at the RX frequency from the PA to the LNA is limited. Once the noise of the transmitter appears at the LNA input, it cannot be filtered out as it is at the same frequency as the wanted signal, so the only option is to reduce the noise of the transmitter. Traditionally, a SAW filter is used between the transmitter IC and the PA. Removing the need for the filter would be desirable, especially in multi-band applications. This has been suggested previously [3], but the best transmitters presented to date have been too noisy ( $-152\text{dBc/Hz}$  [1] and  $-151\text{dBc/Hz}$  [2, 3]) to permit this in a class 3 handset ( $+24\text{dBm}$  TX), using common duplexers (which may only guarantee  $45\text{dB}$  TX-to-RX isolation at the RX frequency), whilst achieving a competitive RX noise figure.

To calculate a realistic noise target, the following assumptions are made: PA output power is  $+27\text{dBm}$ , noise at the RX frequency due to the PA itself is  $-139\text{dBm/Hz}$  at the PA output, duplexer isolation from PA to LNA is  $45\text{dB}$  at the RX frequency, and the worst-case RX noise figure is  $3.3\text{dB}$  referred to the LNA input without transmitter noise. In order to keep the worst-case RX noise figure referred to the LNA input under  $4\text{dB}$ , the noise of the transmitter must be under  $-162\text{dBc/Hz}$  at the IC output.

In this direct-conversion transmitter, to prevent the RF output from affecting the synthesiser VCO, the VCO runs at nominally  $4\text{GHz}$  where the nominal carrier frequency is  $2\text{GHz}$ . The modulator needs a divider to generate the  $2\text{GHz}$  LO signal. The LO divider is only one of many noise sources in a conventional transmitter, but it is quite difficult to design a divider which produces output phase noise much lower than  $-163\text{dBc/Hz}$ . Instead, in this work, a modulator topology is used that suppresses LO divider phase noise.

The modulator accepts a quadrature (I/Q) baseband input, supplied differentially and denoted by I, IB, Q, and QB. Each of these four baseband signals is upconverted separately and the output currents are combined at RF. Figure 19.1.1 depicts one quarter of an I/Q modulator, specifically the section for the positive I baseband signal. Three other similar circuits are used for the IB, Q, and QB baseband inputs, however their LO signals are exchanged in order to create the correct phase relationship to make a complete I/Q modulator.

In Fig. 19.1.1, the  $g_m$  stage of the modulator is formed by NMOS device MN0 with a source degeneration resistor and an opamp to make the transfer function more linear. The current from the  $g_m$  stage is fed to a differential pair of devices MN1 and MN2, switched at  $4\text{GHz}$  by signals VLO and VLOB. This pair steers the current between two further differential pairs. The pair MN3 and MN4 is switched by  $2\text{GHz}$  LO signals LOI and LOIB, whereas the pair MN5 and MN6 is switched in quadrature by the signals LOQ and LOQB. This circuit is most easily understood by stepping through the LO waveforms of Fig. 19.1.2. The timing of the  $2\text{GHz}$  LO relative to the  $4\text{GHz}$  LO is such that whenever one of the  $2\text{GHz}$  LO signals changes state, at that time there is no current flowing through the associated differential pair. Although the baseband current is switched between the output terminals at a rate of  $2\text{GHz}$ , the time of switching is determined only by the  $4\text{GHz}$  LO signal. In this way the modulator rejects timing inaccuracies such as quadrature error and phase noise in the  $2\text{GHz}$  LO

signals. For the ideal waveforms in Fig. 19.1.2, the timing alignment between the  $4\text{GHz}$  and  $2\text{GHz}$  LO signals only has to be accurate to within a half period of the  $4\text{GHz}$  LO, but in reality the alignment has to be more precise to allow for quadrature errors in the  $2\text{GHz}$  LO signals and finite slew rate in all LO signals. The measured output noise for different phase offsets between the  $2\text{GHz}$  and  $4\text{GHz}$  LO signals is shown in Fig. 19.1.4, using an adjustable phase shifter in the  $2\text{GHz}$  LO path. The output noise is better than  $-162\text{dBc/Hz}$  over a  $45^\circ$  window, typically producing  $-163\text{dBc/Hz}$  after auto-calibration.

To provide enough RF power (and to overcome SAW filter losses), existing direct-conversion transmitters use a modulator followed by a driver amplifier. When low noise is the objective and total supply current is limited, having a driver amplifier is undesirable because it reduces the current available for use in the modulator and also makes the required noise specification of the modulator tougher. On the other hand, doubling the current used in the modulator decreases the noise by  $3\text{dB}$  (when expressed in  $\text{dBc/Hz}$ ), and provides  $3\text{dB}$  more output power. In this transmitter, 8 identical I/Q modulator stages are connected in parallel. The modulator output is differential but using an on-chip balun, a single-ended  $50\Omega$  output is provided to the PA. The measured return loss is better than  $10\text{dB}$  from  $1710$  to  $2025\text{MHz}$ . To obtain up to  $18\text{dB}$  of RF gain control, some of the 8 modulators may be turned off. If further gain reduction is needed, then all of the 8 modulators are turned off and another separate modulator is turned on instead, this extra modulator being coupled to the balun through a  $6\text{dB}$  resistive attenuator. Further attenuator stages are provided to create an R-2R ladder as shown in Fig. 19.1.3. During low-power transmission, only one of the 7 modulators connected to taps on the R-2R ladder will be active, resulting in a low power consumption. When each modulator section is turned off, its branch of the  $2\text{GHz}$  LO distribution tree is turned off to prevent any carrier leakage by that path. When the RF gain control range has been exhausted, the baseband signals are attenuated to give further gain control. As  $>60\text{dB}$  of gain control occurs at RF, trimming the DC offset of the baseband circuits is unnecessary.

Transmitting  $+3.8\text{dBm}$  at  $1950\text{MHz}$ , noise at  $2140\text{MHz}$  is  $-163\text{dBc/Hz}$ , ACLR is  $-46\text{dBc}$  (see Fig. 19.1.5), EVM is  $3.7\%$  and the supply current is  $84\text{mA}$ . The supply current decreases rapidly with output power, e.g., at  $0\text{dBm}$  the supply current is  $65\text{mA}$ , and at  $-20\text{dBm}$  or lower the supply current is  $27\text{mA}$ . In typical use, maximum transmit power only occurs for a small percentage of the time [4] and the weighted average supply current of this TX is therefore about  $35\text{mA}$ . Transmitting on  $1920\text{MHz}$ , the noise at  $1880\text{MHz}$  is  $-158\text{dBc/Hz}$ , preventing interference to the DCS band without needing a SAW filter. The output balun provides some filtering so that harmonic signals (at  $4\text{GHz}$ ,  $6\text{GHz}$ , etc.) are all below  $-40\text{dBc}$  and require no more filtering than already provided to suppress PA harmonics. A summary of performance is shown in Fig. 19.1.6, and a die micrograph of the modulator (occupying  $0.8\text{mm}^2$ ) is shown as Fig. 19.1.7.

### References:

- [1] R. Koller, T. Ruhlicke, D. Pimingsdorfer, and B. Adler, "A Single-chip  $0.13\mu\text{m}$  CMOS UMTS W-CDMA Multi-band Transceiver," *IEEE RFIC Symp. Dig. Papers*, pp. 187-190, June, 2006.
- [2] G. Brenna, D. Tschopp, and Q. Huang, "Carrier Leakage Suppression in Direct-Conversion WCDMA Transmitters," *ISSCC Dig. Tech. Papers*, pp. 270-271, Feb., 2003.
- [3] G. Brenna, D. Tschopp, J. Rogin, et al. "A  $2\text{-GHz}$  Carrier Leakage Calibrated Direct-Conversion WCDMA Transmitter in  $0.13\mu\text{m}$  CMOS," *IEEE J. Solid-State Circuits*, Vol. 39, pp. 1253-1262, Aug., 2004.
- [4] V. W. Leung, L.E. Larson, and P.S. Gudem, "Digital-IF WCDMA Handset Transmitter IC in  $0.25\mu\text{m}$  SiGe BiCMOS," *IEEE J. Solid-State Circuits*, vol. 39, pp. 2215-2225, Dec., 2004.
- [5] H. Tomiyama, C. Nishi, N. Ozawa, et al. "A Low Voltage ( $1.8\text{V}$ ) Operation Triple Band WCDMA Transceiver IC," *IEEE RFIC Symp. Dig. Papers*, pp. 165-168, June, 2006.
- [6] D. Kaczman, C. Dozier, N. Godambe, et al., "A Tri-Band ( $2100/1900/800\text{MHz}$ ) Single-Chip Cellular Transceiver for WCDMA/HSDPA," *IEEE RFIC Symp. Dig. Papers*, pp. 281-284, June, 2005.

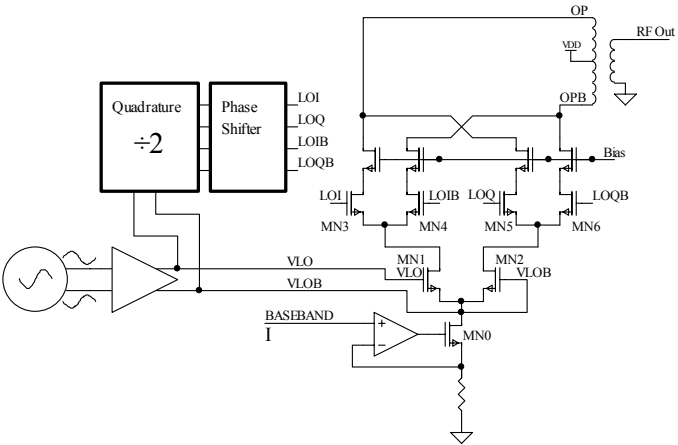


Figure 19.1.1: Topology of the modulator core (one quarter of an I/Q Modulator).

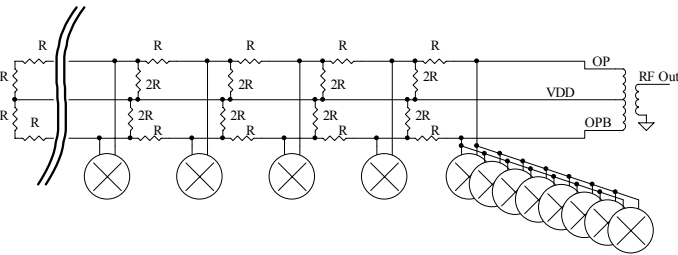


Figure 19.1.3: RF gain control arrangement using many modulator stages.

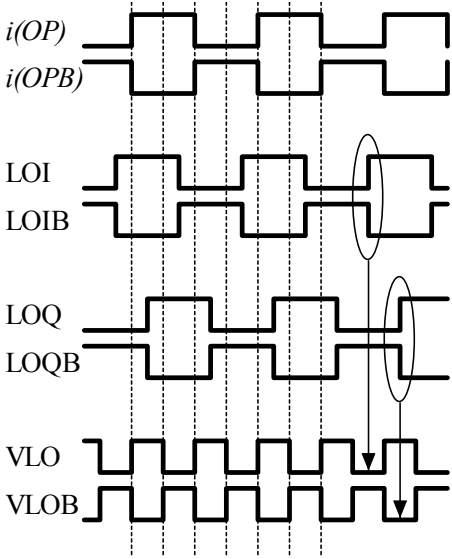


Figure 19.1.2: Phase relationship between 2GHz and 4GHz LO waveforms.

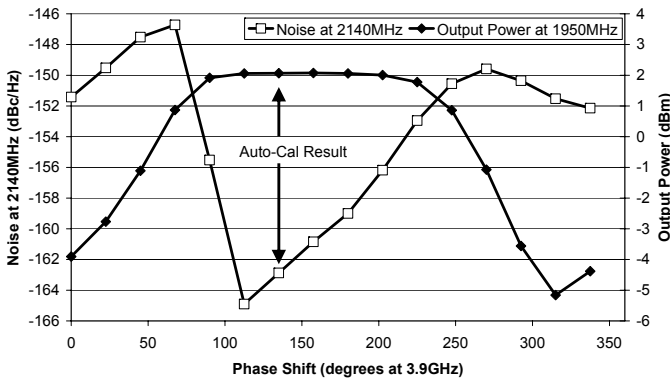


Figure 19.1.4: Effect of adjusting phase of 2GHz LO relative to 4GHz LO.

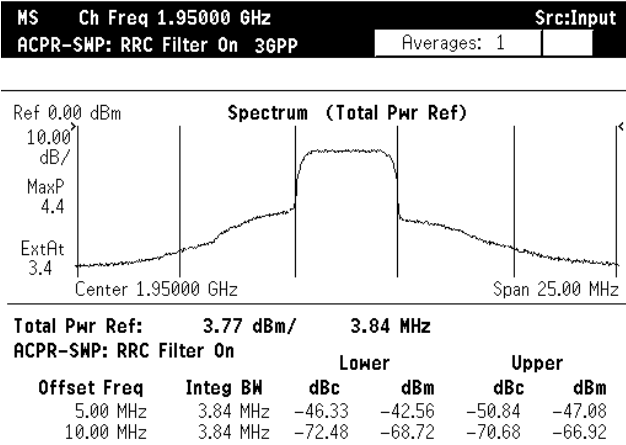


Figure 19.1.5: Typical ACLR performance.

Design	Process	ACLR (dB)	@ Power (dBm)	Noise (dBm/Hz)	Noise (dBc/Hz)	@ Offset (MHz)	Power Supply
[1]	0.13µm CMOS	-44	10.75		-152	190	26 to 80mA 2.7V
[2]	0.13µm CMOS	-38	2.5	-149	(-151.5) inferred	190	45mA 1.5V
[5]	0.18µm SiGe BiCMOS	-38	0	-140.9	(-140.9) inferred	Rx band	(IC) 31 to 53mA 1.8V
[6]	0.35µm SiGe:C BiCMOS	-46	9.5	-132	(-141.5) inferred	130	(IC) 49 to 64mA 2.775V
This Work	0.18µm CMOS	-46	3.8		-163	190	27 to 84mA 2.8V

Figure 19.1.6: Performance summary and comparison.

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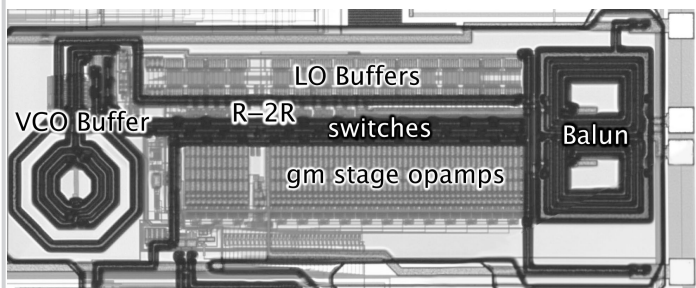


Figure 19.1.7: Die micrograph.